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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/541,465	07/06/2005	Shinji E. Mino	L7990.05102	8930

52989 7590 11/29/2006

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EXAMINER	
ARORA, AJAY	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 11/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/541,465	MINO ET AL.	
	Examiner	Art Unit	
	Ajay K. Arora	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 6-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 6-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 and 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bates (US 5,338,625), hereinafter Bates, in view of Rezvani (US 6,663,037), hereinafter Rezvani.

Regarding Claim 1, Bates (refer to Figure 1 and 3) teaches a battery mounted integrated circuit device, comprising: (1) a semiconductor substrate (22); (2) a solid state battery (10) mounted on said semiconductor substrate (Col. 3, lines 23-27); (3) an integrated circuit (16) mounted on said semiconductor substrate; said solid state battery (refer to Figure 3) comprising a positive electrode, a negative electrode (cathode 24 and anode 28), and a solid electrolyte (26) disposed between said positive electrode and said negative electrode. However, Bates does not teach the claimed first and second diffusion layers and their configuration. Rezvani teaches a method for isolating circuits in one region of the substrate (110) from another region of the substrate (120) using substrate n-wells, wherein the isolation structure comprises: a first diffusion layer (140),

containing an N-type impurity, formed between a first region (110) of semiconductor substrate and another region (120) of the semiconductor substrate; and a second diffusion layer (130), containing an N-type impurity, formed below said region (140) of said semiconductor substrate, and overlapping with said first diffusion layer. Figure 1B of Rezvani further teaches that the concentration of said N-type impurity (n+) in said first diffusion layer (140) is higher than the concentration of said N-type impurity (n) in said second diffusion layer (140). Further, Rezvani (see Figure 4B) teaches that the said first diffusion layer and said second diffusion layer have a positive potential (Col. 6, lines 28-39) and still further teaches that during operation of the device, the said positive potential is not less than a potential of said positive electrode with respect to said negative electrode (Col. 4, lines 1-6).

It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the invention of Bates with the isolation structure of Rezvani so that the battery mounted integrated circuit device includes a first diffusion layer, containing an N-type impurity, formed between a region of said semiconductor substrate where said solid state battery is mounted and an region of said semiconductor substrate where said integrated circuit is mounted; and a second diffusion layer, containing an N-type impurity, formed below said region of said semiconductor substrate where said solid state battery is mounted, and overlapping with said first diffusion layer, and further that the concentration of said N-type impurity in said first diffusion layer is higher than the concentration of said N-type impurity in said second diffusion layer, such that at least

when said battery is being charged and discharged, the said first diffusion layer and said second diffusion layer have a positive potential not less than a potential of said positive electrode with respect to said negative electrode. The ordinary artisan would have been motivated to modify Bates for at least the purpose of fabricating circuits of diverse functionality (such as a solid state thin film battery and an analog IC) on a single integrated circuit (see Rezvani, Col. 1, lines 10-13), while enabling isolation/shielding between the two (see Rezvani, Col. 1, lines 47-50).

Note that as explained above, Rezvani teaches that during device operation, the said first diffusion layer and said second diffusion layer have a positive potential, the said positive potential is not less than a potential of said positive electrode with respect to said negative electrode. Therefore, the device of Bates modified by Rezvani as above will have the above characteristics during device operation, i.e. including when said solid state battery is being charged and discharged.

Regarding Claims 2 and 3, Rezvani teaches a high concentration of said N-type impurity in said first diffusion layer (higher than second diffusion layer) but does not expressly teach that: a) the concentration is not less than 1×10^{19} atoms/cm^3 (as in Claim 2), or b). that the ratio of the concentration of said N-type impurity in said first diffusion layer to the concentration of said N-type impurity in said second diffusion layer is not less than 1×10^{1} and not more than 1×10^{5} (as in Claim 3). However, Rezvani

teaches that among other things, the concentration of said N-type impurity and the relative concentration of N-impurity in first and second diffusion layers affects isolation achieved and that various doping schemes may be used (Col. 3, lines 38-58). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the invention of Bates so that: a) the concentration of said N-type impurity in said first diffusion layer is not less than 1×10^{19} atoms/ cm^3 and/or b). that the ratio of the concentration of said N-type impurity in said first diffusion layer to the concentration of said N-type impurity in said second diffusion layer is not less than 1×10^{1} and not more than 1×10^{5}. The ordinary artisan would have been motivated to modify Bates for at least the purpose of design considerations to achieve optimal isolation for the specific devices being isolated and their associated circuit parameters like operating voltage and breakdown voltage.

Regarding Claim 6, Rezvani (see Figure 1A and 1B) teaches that said first diffusion layer (140) surrounds the region (110) to be isolated, which can be the region where solid state battery is mounted (as explained for Claim 1).

Regarding Claim 7, Rezvani (see Figure 1B) teaches the battery mounted integrated circuit device further comprising a wiring layer (wiring connected to 180) for connecting said first diffusion layer (140) with the outside.

Regarding Claim 8, Rezvani (see Figure 1B) teaches a potential controlling section (180) for controlling a potential to be applied to said first diffusion layer and said second diffusion layer.

Response to Arguments

Applicant's arguments filed 09/14/06 have been fully considered but they are not persuasive.

On page 6, applicant argues about the rejection of claim 1 that "Since the first diffusion layer and the second diffusion layer overlap each other, the solid state battery region is completely surrounded by the first diffusion layer and the second diffusion layer". This argument is not persuasive. As recited in claim 1, the overlap between first diffusion layer and the second diffusion layer may be to any extent, and hence it cannot be concluded that the solid state battery region is completely surrounded by the first diffusion layer and the second diffusion layer.

On page 7, applicant argues "Rezvani does not disclose or suggest mounting a solid state battery on a semiconductor substrate". In response to applicant's above argument against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references (in the instant case, Bates in view of Rezvani). See *In re Keller*, 642 F.2d 413, 208

USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "Rezvani does not disclose or suggest providing an n-well below the quiet region" as stated on page 7; "Rezvani does not disclose or suggest providing the n-well over the entire semiconductor substrate between the quiet region and the noisy region", as stated on page 7-8; and "the effect achieved by the claimed invention of preventing cation diffusion into the IC region is not suggested by the applied references", as stated on page 8) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, applicant argues that "Office action fails to indicate why a skilled artisan would be motivated to prevent

noise produced by an integrated circuit from reaching a battery". This argument is not persuasive. If the noise produced by an integrated circuit reaches a battery, the noise can pollute the battery voltage which may become unsuitable for other components connected to the battery. This is in the knowledge generally available to one of ordinary skill in the art, as evidenced by supporting NPL reference titled "Circuit Tradeoffs Minimize Noise in Battery-Input Power Supplies" (see 1st page, paragraph immediately following the subtitle "Types of Noise") provided with this office action.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ajay K. Arora whose telephone number is (571) 272-8347. The examiner can normally be reached on Mon through Fri, 8am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Douglas W. Owens 11/24/06

DOUGLAS W. OWENS
PRIMARY EXAMINER